ABSTRACT:

To provide a circuit arrangement for converting a preferably analog input signal from at least a receiver, particularly at least a UHF or VHF receiver, into a digital output signal, said circuit arrangement (100) comprising:

at least one threshold value circuit (30) having a first input (32) for receiving the input signal; a second input (34) for receiving a reference threshold signal generated by at least one reference threshold signal detector (20); and an output (36),

the digital output signal being formed in the threshold value circuit (30) by comparing the input signal at the first input (32) with the reference threshold signal at the second input (34);

at least one detector circuit (40) arranged subsequent to and communicating with the threshold value circuit (30) for detecting overshoots and/or pauses and/or interruptions in the input signal; and

at least one control circuit (50) communicating with the detector circuit (40) and the reference threshold signal detector (20), the output signal of said control circuit ensuring that the reference threshold signal applied to the threshold value circuit (30) during time intervals (T_{aus}) that are assignable to the overshoots and/or the pauses and/or the interruptions detected by the detector circuit (40) is maintained at approximately the reference threshold value comprising the reference threshold signal at the start of the overshoot and/or the pause and/or the interruption,

by which pulse width distortions are reduced and losses of single bits, particularly at the start of a data packet, are obviated, and by which digital noise at the data output is prevented, it is proposed that

the reference threshold signal detector (20) forms the reference threshold signal from the input signal and comprises at least a resistor (22) having a variable resistance value (R) and at least a capacitive element (24) having a capacitance (C) arranged subsequent to the resistor (22), and that

the resistor (22) assumes a high-ohmic state preventing a discharge of the capacitive element (24) during the time intervals (T_{aus}) that are assignable to the overshoots and/or the pauses and/or the interruptions, and a low-ohmic state during the time intervals that are not assignable to the overshoots and/or the pauses and/or the interruptions. Fig.1